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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/766,217	01/27/2004	Daniel C. Guterman	SAND-01011US0	3316

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EXAMINER	
HUR, JUNG H	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 06/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/766,217	GUTERMAN ET AL.	
	Examiner	Art Unit	
	Jung (John) Hur	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-12,24-35 and 40-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1,3-12,43 and 45-47* is/are allowed.

6)☒ Claim(s) *24,26-32,34,35,40 and 44* is/are rejected.

7)☒ Claim(s) *25,33,41 and 42* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 March 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Amendment

1. Acknowledgment is made of applicant's Amendment, filed 06 March 2006. The changes and remarks disclosed therein have been considered.

Claim 2 has been cancelled, and claims 40-47 have been added by Amendment. Therefore, claims 1, 3-12, 24-35 and 40-47 are pending in the application.

Specification

2. Claims 44 and 47 are objected to because of the following informalities:

In claim 44, line 7, "signal" appears to be in error, and should be removed.

The status of claim 47 should be --new--.

Appropriate correction is required.

Drawings

3. The replacement drawing sheet for Figs. 1-3 was received on 06 March 2006. The drawings in the replacement sheet are acceptable.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 24, 26-29, 31, 40 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wong et al. (U.S. Pat. No. 5,969,986) in view of Holzmann et al. (U.S. Pat. No. 6,301,161).

Regarding claim 24, Wong, for example in Figs. 1 and 2, discloses a method for programming non-volatile storage elements (memory arrays 130 in Fig. 1), comprising: providing a common programming signal (for example, Vpp, which is common to all arrays) to said non-volatile storage elements (via 124, 126, 138 and 132), said step of providing is part of a programming process that includes a first programming phase (associated with one of the PIPELINE write cycles in Fig. 2) and a second programming phase (associated with another one of the PIPELINE write cycles in Fig. 2) such that one or more of said non-volatile storage elements are in said first programming phase while one or more of said non-volatile storage elements are in said second programming phase (see Fig. 2, which shows that the PIPELINE write cycles are staggered and overlap); and performing first verification (associated with the one of the PIPELINE write cycles) for said one or more of said non-volatile storage elements that are in said first programming phase while concurrently performing second verification (associated with the another one of the PIPELINE write cycles) for said one or more of said non-volatile storage elements that are in said second programming phase (see Fig. 2, for staggered and overlapping PIPELINE write cycles).

Wong does not disclose that the first programming phase/verification is a coarse programming phase/verification and that the second programming phase/verification is a fine programming phase/verification.

Holzmann, for example in Figs 3 and 5, discloses a programming/write cycle comprising coarse programming phase and verification (including steps 310-330 in Fig. 3) followed by fine programming phase and verification (steps 340-360; see also Fig. 5).

Since use of coarse and fine programming phases and verifications in flash memories were common and well known in the art (as exemplified in Holzmann), it would have been obvious at the time the invention was made to a person having ordinary skill in the art to implement the coarse-fine programming phases and verifications (as in Holzmann) for the programming/write cycles of Wong, such that one PIPELINE is in a coarse programming phase and verification during its write cycle concurrently while another PIPELINE is in a fine programming phase and verification during its write cycle (since the write cycles are staggered and overlap in Fig. 2 of Wong), for the purpose of providing an efficient and accurate means for programming a pipelined flash memory (see for example Holzmann, column 1, lines 38-40).

Regarding claims 26-29, 31 and 40, the above Wong/Holzmann combination further discloses that said non-volatile storage elements are multi-state flash memory devices (see for example Wong, Fig. 6 and its brief description, and column 3, line 60 through column 4, line 12);

using said coarse verification to determine when a particular non-volatile storage element completes said coarse programming phase (step 330 in Fig. 3 of Holzmann) and causing said particular non-volatile storage element to begin said fine programming phase (step 340 in Fig. 3 of Holzmann);

wherein: following said non-volatile storage element beginning said fine programming phase, said non-volatile storage element begins said fine verification (step 360 in Fig. 3 of Holzmann);

wherein said step of performing comprises: performing coarse verification for said particular non-volatile storage element without performing fine verification for said particular non-volatile storage element, if said particular non-volatile storage element is determined to be in said coarse programming phase (Fig. 3 of Holzmann shows that coarse and fine phases are performed sequentially and separately for a given storage element); and performing fine verification for said particular non-volatile storage element without performing coarse verification for said particular non-volatile storage element, if said particular non-volatile storage element is determined to be in said fine programming phase (similarly, Fig. 3 of Holzmann shows that coarse and fine phases are performed sequentially and separately for a given storage element);

wherein said step of providing includes providing said common programming signal to steering gates (including 124, 126, 138 and 132 in Fig. 1 of Wong).

Regarding claim 44, Wong, for example in Figs. 1, 2 and 6, discloses an apparatus for programming non-volatile storage elements (memory arrays 130 in Fig. 1), comprising: a programming circuit (including 150 generating Vpp) in communication with said non-volatile storage elements, said programming circuit provides a common program signal (for example, Vpp, which is common to all arrays) to said non-volatile storage elements; and one or more verification selection circuits (including 150 generating Vvfy and sense amplifiers 136) in

communication with said non-volatile storage elements, said one or more verification selection circuits cause a first subset of said non-volatile storage elements (for example, any one of memory arrays 130 in Fig. 1) to be subjected to first verification (associated with one of the PIPELINE write cycles in Fig. 2, corresponding to one of the memory arrays 130) concurrently while a second subset of said non-volatile storage elements (for example, another one of memory arrays 130 in Fig. 1) are subjected to second verification (associated with another one of the PIPELINE write cycles in Fig. 2, corresponding to another one of the memory arrays 130; in Fig. 2, the PIPELINE write cycles overlap in time).

Wong does not disclose that the first verification is coarse verification and the second verification is fine verification.

Holzmann, for example in Figs 3 and 5, discloses a write cycle comprising coarse verification (including steps 310-330 in Fig. 3) followed by fine verification (steps 340-360; see also Fig. 5).

Since use of coarse and fine programming/verification in flash memories were common and well known in the art (as exemplified in Holzmann), it would have been obvious at the time the invention was made to a person having ordinary skill in the art to implement the coarse-fine programming/verification technique (as in Holzmann) for the write cycles of Wong, such that one PIPELINE is subjected to a coarse verification during its write cycle concurrently while another PIPELINE is subjected to a fine verification during its write cycle (since the write cycles are staggered and overlap in time in Fig. 2 of Wong), for the purpose of providing an efficient and accurate means for programming a pipelined flash memory (see for example Holzmann, column 1, lines 38-40; see also Holzmann Fig. 2).

6. Claims 30, 32, 34 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wong et al. in view of Holzmann et al. as applied to claims 24 and 28 above, and further in view of Guterman et al. (U.S. Pat. No. 6,222,762).

Regarding claims 30 and 32, the above Wong/Holzmann combination discloses an apparatus and a method according to claims 24 and 28, with the exception of said coarse reference signal and said fine reference signal providing reference currents; said coarse reference signal and said fine reference signal providing an indication of discharge times; said coarse verification and said fine verification being performed using a discharge method; causing said particular non-volatile storage element to begin said fine programming phase includes raising a bit line voltage; or said coarse verification and said fine verification are based on a bit line discharge process.

Guterman, for example in Figs. 1-3, discloses a reference signal providing a reference current (306 in Fig. 3, as an alternative to a reference voltage in Fig. 2); a reference signal providing an indication of discharge times (indicated by TSENSE in Fig. 1b); a verification being performed using a discharge method (see Figs. 1a and 1b); causing a particular non-volatile storage element to begin a programming phase including raising a bit line voltage (see Figs. 1a and 1b, in which the voltage on the bit line 101 is raised or pre-charged); and a verification are based on a bit line discharge process (see Figs. 1a and 1b).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to use the bit line discharge means of Guterman, as an alternative equivalent means for a flash memory verifying operation, adapted for the coarse-fine techniques

of Holzmann, such that discharge related measurements will be compared with a coarse reference value during a coarse phase and with a fine reference value during a fine phase (similar to those of Holzmann), for the purpose of providing reading/verifying means that is flexible, consistent, adaptable and capable of covering a wide dynamic range (see for example, Guterman, column 1, lines 55-58).

Regarding claim 34, the above Wong/Holzmann combination discloses a method according to claim 24, with the exception of said step of performing comprising: pre-charging a first bit line for a first non-volatile storage element; applying a verify signal to a control gate for said first non-volatile storage element; determining a time for said bit line to discharge until a voltage or a current of said bit line reaches a predetermined value; comparing a coarse compare value to said time, if said first non-volatile storage element is in said coarse programming phase; and comparing a fine compare value to said time, if said first non-volatile storage element is in said fine programming phase.

Guterman, for example in Figs. 1-3, discloses pre-charging a first bit line for a first non-volatile storage element (see Figs. 1a and 1b, in which the bit line 101 is pre-charged); applying a verify signal to a control gate (via the word line 103) for said first non-volatile storage element (to initiate a discharge; see Fig. 1b and column 4, lines 31-48); determining a time for said bit line to discharge until a voltage or a current of said bit line reaches a predetermined value (VREF in Fig. 1b).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to use the bit line discharge means of Guterman, as an alternative

equivalent means for a flash memory verifying operation, adapted for the coarse-fine techniques of Holzmann, such that discharge related measurements would be compared with a coarse reference value during a coarse phase and with a fine reference value during a fine phase (similar to those of Holzmann), for the purpose of providing reading/verifying means that is flexible, consistent, adaptable and capable of covering a wide dynamic range (see for example, Guterman, column 1, lines 55-58).

Regarding claims 35, the above Wong/Holzmann/Guterman combination further discloses that said predetermined value is a first value if said first non-volatile storage element is in said coarse programming phase (i.e., in the above combination, with Guterman's verifying means adapted for the coarse-fine verification, as in Holzmann, the reference voltage/current would have a coarse value during the coarse phase); and said predetermined value is a second value if said first non-volatile storage element is in said fine programming phase (i.e., in the above combination, with Guterman's verifying means adapted for the coarse-fine verification, as in Holzmann, the reference voltage/current would have a fine value during the fine phase).

Allowable Subject Matter

7. Claims 1, 3-12, 43 and 45-47 are allowed.

Claims 25, 33, 41 and 42 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 1, the prior arts of record do not disclose or suggest an apparatus as recited in claim 1, and particularly, a first subset of said non-volatile storage elements connected to said common control line to be subjected to coarse verification concurrently while a second subset of said non-volatile storage elements connected to said common control line are subjected to fine verification.

Regarding claims 25 and 33, the record of the prosecution as a whole makes clear the reasons for the indication of allowable subject matter. See the previous Office Action.

Regarding claims 41 and 42, the prior arts of record do not disclose or suggest a method as recited in claim 41 or 42, and particularly, said non-volatile storage elements being connected to a common control line or a common word line.

Regarding claims 45 and 47, the prior arts of record do not disclose or suggest an apparatus or a method as recited in claim 45 or 47, and particularly, the non-volatile storage elements are programmed together as part of a common coarse/fine programming process, and a first subset of said non-volatile storage elements being subjected to coarse verification concurrently while a second subset of non-volatile storage elements are subjected to fine verification.

Regarding claim 46, the prior arts of record do not disclose or suggest an apparatus as recited in claim 46, and particularly, a first subset of said array of non-volatile storage elements being subjected to coarse verification concurrently while a second subset of said array of non-volatile storage elements are subjected to fine verification.

Response to Arguments

8. Applicant's arguments, see starting on page 10, filed 06 March 2006, with respect to claim 1 have been fully considered and are persuasive. The 35 USC 103 rejection of claim 1 (and its dependent claims) has been withdrawn.

9. Applicant's arguments, filed 06 March 2006, with respect to claims 24 and 44 have been fully considered but they are not persuasive.

Regarding claim 24, Applicant argues, in the middle paragraph on page 12, that "[t]he non-volatile storage elements in the different memory arrays do not receive a common programming signal." Similar arguments are presented on page 13 with respect to claim 44.

In response, it is noted that Wong, in Fig. 1, does disclose that the non-volatile storage elements in the different memory arrays (103-1, 103-2, etc.) receive a common programming signal (for example, Vpp; i.e., Vpp is a programming signal for all the arrays, thus common to all the arrays).

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jung (John) Hur whose telephone number is (571) 272-1870. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

jhh

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